SELF-ALIGNED METAL-OXIDE-COMPOUND SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION

Field of the Invention

The present invention pertains to compound semiconductor field effect devices and more specifically to enhancement mode self-aligned metal-oxide-compound semiconductor transistors and methods of fabrication.

Background of the Invention

Metal-oxide-semiconductor field effect transistors (MOSFET) are the workhorse of the silicon (Si) semiconductor industry. The rapid advance of portable electronic systems and the exponential increase in integration density has spurred the transition to low-power technologies. Reduction of the supply voltage is key for reducing power dissipation. At the present time, Si CMOS offers significant advantages in terms of integration level and cost; however, reductions in circuit speed of scaled Si CMOS (including SOI) are anticipated as the power supply is reduced to 1V or below. In contrast to Si, complementary GaAs exhibits optimum speed/power performance and efficiency at a low supply voltage of 1 V and below.

For compound semiconductors, prior art comprises the use of a metal-semiconductor junction as a gate electrode in field effect transistors instead of the standard metal-oxide-semiconductor junction employed in Si technology. The use of a metal semiconductor junction, however, results in excessive leakage current, high power dissipation, reduced logic swing, reduced design flexibility, and limited device performance. Consequently, optimum device performance and high IC integration levels could not be realized and commercial marketability has been limited.

Thus what is needed are new and improved compound semiconductor devices and methods of fabrication which overcome these problems. What is also needed are new and improved compound semiconductor field effect transistors (FET). What is also needed are new and improved compound semiconductor FETs using metal-oxide-semiconductor junctions (MOSFET). What is also needed are new and improved compound semiconductor MOSFETs using a self-aligned gate structure. What is also needed are new and improved self-aligned compound semiconductor MOSFETs using enhancement mode operation. What is also needed are new and improved self-aligned compound semiconductor MOSFETs with stable and reliable device operation. What is also needed are new and improved self-aligned compound semiconductor MOSFETs which enable optimum compound semiconductor device performance. What is also needed are new and improved self-aligned compound semiconductor MOSFETs with optimum efficiency and output power for RF and microwave applications. What is also needed are new and improved self-aligned compound semiconductor MOSFETs for use in complementary circuits and architectures. What is also needed are new and improved self-aligned compound semiconductor MOSFETs for low power/high performance complementary circuits and architectures. What is also needed are new and improved self-aligned compound semiconductor MOSFETs which offer the design flexibility of complementary architectures. What is also needed are new and improved self-aligned compound semiconductor MOSFETs which keep interconnection delays in ULSI under control.

What is also needed are new and improved methods of fabrication of self-aligned compound semiconductor MOSFETs. What is also needed is new and improved methods of fabrication of self-aligned compound semiconductor MOSFETs which are compatible with established complementary GaAs heterostructure FETs (CGaAs) technologies. What is also needed are new and improved

compound semiconductor MOSFETs which are relatively easy to fabricate and use.

Brief Description of the Drawings

The invention is pointed out with particularity in the appended claims. However, a more complete understanding of the present invention may be derived by referring to the detailed description and claims when considered in connection with the figures, wherein like reference numbers refer to similar items throughout the figures, and:

FIG. 1 is simplified cross sectional view of a self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention;

FIG. 2 is a graph illustrating measured output characteristics of a p-channel self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention; and

FIG. 3 is a graph illustrating transfer characteristics and transconductance of a p-channel self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention;

FIG. 4 is a graph illustrating predicted performance of optimized self-aligned enhancement mode compound semiconductor MOSFETs in accordance with a preferred embodiment of the present invention; and

FIG. 5 is a simplified flow chart illustrating a method of manufacturing a self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention.

The exemplification set out herein illustrates a preferred embodiment of the invention in one form thereof, and such exemplification is not intended to be construed as limiting in any manner.

Detailed Description of the Drawings

The present invention provides, among other things, a self-aligned enhancement mode metal-oxide-compound semiconductor FET. The FET includes a stoichiometric Ga_2O_3 gate oxide layer positioned on upper surface of a compound semiconductor wafer structure. The stoichiometric Ga_2O_3 layer forms an atomically abrupt interface with the compound semiconductor wafer structure. A refractory metal gate electrode is preferably positioned on upper surface of the stoichiometric Ga_2O_3 gate oxide layer. The refractory metal is stable on the stoichiometric Ga_2O_3 gate oxide layer at elevated temperature. Self-aligned source and drain areas, and source and drain contacts are positioned on the source and drain areas. In a preferred embodiment, the metal-oxide-compound semiconductor transistor includes a stoichiometric Ga_2O_3 gate oxide layer of 40 - 200 Å thickness positioned on upper surface of a compound semiconductor heterostructure. The compound semiconductor heterostructure comprises $Al_xGa_{1-x}As$ and $In_yGa_{1-y}As$ layers which are grown on a compound semiconductor substrate, a refractory metal gate of W, WN, or WSi, self aligned donor (n-channel FET) or acceptor (p-channel FET) implants, and source and drain ohmic contacts.

FIG. 1 is simplified cross sectional view of a self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention. Device 10 includes a compound semiconductor material, such as any III-V material employed in any semiconductor device, represented herein by a III-V semiconductor substrate 11 and a compound semiconductor epitaxial layer structure 12. For the purpose of this disclosure, the substrate 11 and any epitaxial layer structure 12 formed thereon will be referred to simply as a compound semiconductor wafer structure which in FIG. 1 is designated 13. Methods of fabricating semiconductor

wafer structure 13 include, but are not limited to, molecular beam epitaxy (MBE) and metal organic chemical vapor deposition (MOCVD). It will of course be understood that in some specific applications, there may be no epitaxial layers present and upper surface of top layer 15 may simply be the upper surface of substrate 11.

Device 10 further comprises a stoichiometric Ga_2O_3 gate oxide layer 14 positioned on upper surface of top layer 15 of compound semiconductor wafer structure 13 wherein oxide layer 14 forms an atomically abrupt interface 16 with the upper surface of top layer 15. A refractory metal gate electrode 17 which is stable in the presence of Ga_2O_3 at elevated temperature is positioned on upper surface 18 of stoichiometric Ga_2O_3 gate oxide layer 14. Dielectric spacers 26 are positioned to cover the sidewalls of metal gate electrode 17. Source and drain contacts 19 and 20 are deposited on self-aligned source and drain areas 21 and 22, respectively.

In a specific embodiment, the epitaxial layer structure consists of a 5 - 10 Å GaAs top layer 15, a 10 - 100 Å AlGaAs spacer layer 23, a 100 - 250 Å InGaAs channel layer 24, and a GaAs buffer layer 25 grown on a GaAs substrate 11. The separation of the conducting channel forming in layer 24 from interface 16 using spacer layer 23 significantly improves the device reliability and stability and assures optimum device performance. Top GaAs layer 15 is used to form an atomically abrupt Ga_2O_3-GaAs interface with low defect density.

As a simplified example of fabricating a self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of hte present invention, a III-V compound semiconductor wafer structure 13 with an atomically ordered and chemically clean upper surface of top layer 15 is prepared in an ultra-high vacuum semiconductor growth chamber and transferred via a preparation chamber to an oxide deposition chamber. Ga_2O_3 layer 14 is deposited on upper surface of top layer 15

using thermal evaporation from a crystalline Ga_2O_3 source. A refractory metal which is stable on Ga_2O_3 at elevated temperature such as WSi or WN is deposited on upper surface 18 of oxide layer 14 and subsequently patterned using standard lithography. The refractory metal layer is etched until oxide layer 14 is exposed using a refractory metal etching technique such as a fluorine based dry etching process. The refractory metal etching procedure does not etch the oxide layer 14, thus, oxide layer 14 functions as an etch stop layer such that upper surface of top layer 15 remains protected by oxide layer 14. All processing steps are performed using low damage plasma processing. Self-aligned source and drain areas 21 and 22, respectively are realized by ion implantation of Si (n-channel device) and Be/F (p-channel device) using the refractory metal gate electrode 17 and the dielectric spacers 26 as implantation masks. Such ion implantation schemes are compatible with standard processing of complementary heterostructure FET technologies and are well known to those skilled in the art. The implants are activated at 700 °C using rapid thermal annealing such that degradation of the interface 16 established between top layer 15 and oxide layer 14 is excluded. Finally, ohmic source and drain contacts 19 and 20 are deposited on the self-aligned source and drain areas 21 and 22, respectively.

FIG. 2 is a graph illustrating measured output characteristics of a p-channel self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention. FIG. 3 is a graph illustrating transfer characteristics and transconductance of a p-channel self-aligned enhancement mode compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention. In FIG. 2, the measured output characteristics 31, 32, 33, 34, 35, 36, and 37 are shown for a gate voltage V_{GS} = -1, -1.25, -1.5, -1.75, -2, -2.25, and -2.5 V, respectively. In FIG.

3, transfer characteristics 41 and transconductance 42 are shown for a 0.6 μm p-channel self-aligned enhancement mode GaAs based MOS-HFET (metal-oxide-semiconductor heterostructure FET) fabricated according to a preferred embodiment of the present invention. The GaAs based MOS-HFET uses a 150 Å thick $In_{0.2}Ga_{0.8}As$ channel. The oxide thickness is 90 Å. Note that the relative dielectric constant of 10 for Ga_2O_3 yields an equivalent oxide thickness of 35 Å. Including the 100 Å thick $Al_{0.75}Ga_{0.25}As$ spacer layer, the equivalent distance between gate and channel increases to 72 Å. The gate width of the device is 10 μm. The threshold voltage is -0.93 V and a maximum transconductance of 51 mS/mm is measured at V_{GS} = -2.35 V. The threshold voltage and maximum transconductance measured over a 3 inch wafer are -0.93 ± 0.1 V and 46.7 ± 3.9 mS/mm.

FIG. 4 is a graph illustrating predicted performance of optimized self-aligned enhancement mode compound semiconductor MOSFETs in accordance with a preferred embodiment of the present invention. The predicted performance of n- and p-type GaAs based MOS-HFETs fabricated according to a preferred embodiment of the present invention is shown for n-channel devices with 20% In content (curves 51, 52, 53, 54) and 50% or higher In content in the channel (55, 56, 57, 58), and for p-channel devices (59, 60, 61, 62) having a gate length of 1, 0.5, 0.2, and 0.1 μm, respectively. For a physical oxide thickness of 40 Å, a maximum transconductance g_m of ≅ 0.5, 1.3, and 3 S/mm is anticipated at 1 V for p-type devices and n-type devices with 20% and more than 50% In content in the channel, respectively. For maximum g_m, scaling to a minimum feature size of 0.2 μm is apparently sufficient. Note that high g_m of the order of 2 S/mm and higher is of paramount importance for ULSI in order to keep interconnection delay under control.

FIG. 5 is a simplified flow chart illustrating a method of manufacturing a self-aligned enhancement mode

compound semiconductor MOSFET in accordance with a preferred embodiment of the present invention. In step 102, a compound semiconductor wafer structure is provided. In step 104, a stoichiometric Ga_2O_3 gate oxide layer is deposited on upper surface of said compound semiconductor wafer structure. In step 106, a stable refractory gate metal is positioned on upper surface of said stoichiometricGa_2O_3 gate oxide layer. In step 108, source and drain ion implants are provided self-aligned to the gate electrode. In step 110, source and drain ohmic contacts are positined on ion implanted source and drain areas.

In a preferred embodiment, step 102 includes the preparation of an atomically ordered and chemically clean upper surface of the compound semiconductor wafer structure. Step 104 preferably comprises thermal evaporation from a crystalline Ga_2O_3 source on an atomically ordered and chemically clean upper surface of the compound semiconductor wafer structure. The Ga_2O_3 gate oxide layer preferably functions as an etch stop layer such that the upper surface of the compound semiconductor wafer structure remains protected by the gate oxide during and after gate metal etching. The refractory gate metal desirably does not react with or diffuse into the gate oxide layer during high temperature annealing of the self-aligned source and drain ion implants. The quality of the interface formed by the gate oxide layer and the upper surface of the compound semiconductor structure is desirably preserved during high temperature annealing of the self-aligned source and drain ion implants. The self-aligned source and drain implants are desirably annealed at approximately 700 °C using rapid thermal annealing. The self-aligned source and drain implants are desirably realized by positioning dielectric spacers on the sidewalls of the refractory gate metal.

Thus, new and improved compound semiconductor devices and methods of fabrication are disclosed. The new and

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improved self-aligned enhancement mode metal-oxide-compound semiconductor heterostructure field effect transistors enable stable and reliable device operation, provide optimum compound semiconductor device performance for low power/high performance complementary circuits and architectures, keep interconnection delay in ULSI under control, and provide optimum efficiency and output power for RF and microwave applications.

The invention has been described in conjunction with the illustrative embodiment of the invention. As will be apparent to those skilled in the art, various changes and modifications may be made to the above-described embodiment without departing from the spirit or scope of the invention. It is intended that the invention be limited not by the illustrative embodiment, but be limited only by the scope of the claims appended hereto.